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EXAMINER	
KEBEDE, BROOK	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

CT

Office Action Summary	Application No.	Applicant(s)	
	09/678,414	CARLSON, DAVID W.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-7,9,10,13-17,19-25 and 27-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-7,9,10,13-17,19-25 and 27-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. The indicated allowability of claims 9 and 17 is withdrawn in view of the newly discovered reference(s) to Weling et al. (US/5,378,318) and Doan et al. (US/6,331,488). Rejections based on the newly cited reference(s) follow.

Status of the Claims

2. Claims 1, 2, 5-7, 9, 10, 13-17, 19-25 and 27-30 are now pending in the application.

Specification

3. The amendment filed on March 25, 2002 in Paper No. 6 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

Applicant amend in the specification in Paragraph 5, Page 6 as follows: "As shown in Fig. 3C, **a layer material 342 that lowers resistance** is formed over planarized polysilicon layer 340." Although there is support for formation of "the layer of third material over planarized layer material," there is no support for a layer material 342 (i.e., the layer of third material) that lowers resistance as the specification as originally filed. Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 19-22, 23, 25 and 26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 22 recites the limitation "forming a layer of third material on the planarized layer of the first material, **the third layer of material lowering the resistance of the first material**" in lines 13-14. However there is no support for the limitation "**the third layer of material lowering the resistance of the first material**" in the specification as originally filed. Therefore, the subject matter is not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 25 being dependent of claim 24, the selective etching process provides support for selectively etching for the layer of the first material as the specification as originally filed. However, there is no support for the limitation "the layer of third material being selectively etched during selectively etching process" as recited in claim 25. Therefore, there is no support for the limitation "**the layer of third material being selectively etched during selectively etching process**" in the specification as originally filed. Therefore, the subject matter is not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 26 recites the limitation "The method of claim 25 wherein the layer of third material is conductive" in line 1. Although there is support in the specification for the "third material," there is no support for the third material being "conductive" as the specification originally filed. Therefore, there is no support for the limitation "**the layer of third material is conductive**" in the specification as originally filed. Therefore, the subject matter is not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 19, 20, 21, 23 and 26 are also rejected as being dependent of the rejected independent base claim.

Applicant's cooperation is requested in reviewing the claims structure to ensure proper claim construction and to correct any subsequently discovered instances of claim language noncompliance. See *Morton International Inc.*, 28USPQ2d 1190, 1195 (CAFC, 1993).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 2, 5-7, 10, 13-16, 18-25 and 27-30rejected under 35 U.S.C. 102(e) as being anticipate by Li et al. (US/6,162,368).

Re claims 1 and 16, Li et al. disclose a method for forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having spaced-apart wafer

upper levels a wafer lower level that lies between the wafer upper levels, the wafer upper levels lying above the wafer lower level, the method comprising the steps of: forming a layer of first material (16) on the top surface of the wafer (10), the layer of first material (16) having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level; forming a layer of second material (60) on the top surface of the layer of first material (16); and chemically-mechanically polishing the layer of second material (18) and the underlying layer of first material (16) with a slurry until the layer of second material (18) is all removed from the layer of first material (16) to form the planarized layer of material; and wherein the layer of first material makes an electrical contact with a device on the wafer, the planarized layer of material lying over the wafer upper levels and the wafer lower level (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 2, as applied to claim 1 above, Li et al. disclose all the claimed limitations including the limitation wherein the first lower level lies above the wafer upper level (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 5, as applied to claim 1 above, Li et al. disclose all the claimed limitations including the limitation wherein the planarized layer of material has first thickness over the wafer upper level and, wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a second thickness that is equal to or greater than the first thickness (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 6, as applied to claim 1 above, Li et al. disclose all the claimed limitations including the limitation the first material as being polysilicon (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 7, as applied to claim 1 above, Li et al. disclose all the claimed limitations including the limitation the second material is being an oxide (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 10 as applied to claim 2 above, Li et al. disclose all the claimed limitations including the limitation step of forming a layer of third material on the planarized layer of material (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 13, as applied to claim 12 above, Li et al. disclose all the claimed limitations including the limitation wherein the planarized layer of material has first thickness over the wafer upper level and, wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a second thickness that is equal to or greater than the first thickness (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 14, as applied to claim 1 above, Li et al. disclose all the claimed limitations including the limitation the step of doping the layer of first material prior to forming the layer of second material (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 15, as applied to claim 1 above, Li et al. disclose all the claimed limitations including the limitation wherein the layer of first material is doped polysilicon (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 22, Li et al. disclose a method of planarizing a layer of semiconductor material on a processed wafer (10), the wafer having a top surface (not labeled) , the top surface having a wafer lower level (not labeled) and a wafer upper level (not labeled) that lies above the wafer lower level, the method comprising the steps of: forming a layer of first material (16) on the top surface of the wafer (10), the layer of first material (16) having a top surface (not labeled), the

top surface of the layer of first material (16) having a first lower level (not labeled) and a first upper level (not labeled)that lies above the first lower level; forming a layer of second material (18) on the top surface of the layer of first material (16);chemically-mechanically polishing the layer of second material and the underlying layer of first material until the layer of first material is substantially planar to form planarized layer of first material (see Fig. 2D), the planarized layer of first material (16) covering the wafer upper level (not labeled) of the top surface of the wafer (10); and forming a layer of third material (106 or 114) on the planarized layer of the first material (16) (see Fig. 2D), the third layer of material lowering a resistance of the first layer of material (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 19, as applied to claim 22 above, Li et al. disclose all the claimed limitations including the limitation wherein the first lower level lies above the wafer upper level (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 20, as applied to claim 19 above, Li et al. disclose all the claimed limitations including the limitation wherein the planarized layer of material has first thickness over the wafer upper level and, wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a second thickness that is equal to or greater than the first thickness (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 21, as applied to claim 22 above, Li et al. disclose all the claimed limitations including the limitation wherein the first material is doped polysilicon (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 23, as applied to claim 22 above, Li et al. disclose all the claimed limitations including the limitation wherein the layer of first material makes an electrical contact with a device on the wafer (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 24, Li et al. disclose a method for forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having spaced-apart wafer upper levels a wafer lower level that lies between the wafer upper levels, the wafer upper levels lying above the wafer lower level, the method comprising the steps of: forming a layer of first material (16) on the top surface of the wafer (10), the layer of first material (16) having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level; forming a layer of second material (60) on the top surface of the layer of first material (16); and chemically-mechanically polishing the layer of second material (18) and the underlying layer of first material (16) with a slurry until the layer of second material (18) is all removed from the layer of first material (16) to form the planarized layer of material; and wherein the layer of first material makes an electrical contact with a device on the wafer, the planarized layer of material lying over the wafer upper levels and the wafer lower level; selectively etching the planarized layer of material that covers (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 25, as applied to claim 24 above, Li et al. disclose all the claimed limitations including the limitation the step of forming a layer of third material on the planarized layer of material, the layer of third material and the layer of first material being selectively etched during the selectively etching step (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 27, as applied to claim 24 above, Li et al. disclose all the claimed limitations including the limitation wherein the layer of first material and the layer of second material are etched with a slurry that etches the layer of first material and the layer of second material at approximately a same rate (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 28, as applied to claim 24 above, Lin et al. disclose all the claimed limitations including the limitation wherein all of the layer of second material is removed during the chemically-mechanically polishing step (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 29, Li et al. disclose A method for planarizing a material layer on a processed wafer, the wafer having a top surface, the top surface; having spaced-apart wafer upper levels and a wafer lower level that lies between the wafer upper levels, the wafer upper levels lying above the wafer lower level, the method comprising the steps of forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level; forming a layer of second material on the top surface of the layer of first material; and forming a planarized layer of material by chemically-mechanically polishing the layer of second material and the underlying layer of first material with a slurry until the layer of second material is substantially all removed from the layer of first material, the planarized layer of material lying over the wafer upper levels and the wafer lower level see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 30, Li et al. disclose a method of planarizing a layer of semiconductor material on a processed wafer, the wafer having a top surface, the top surface having a wafer lower level and a wafer upper level that lies above the wafer lower level, the method comprising the steps of: forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level; forming a layer of second material on the top surface of the layer of first material; chemically-mechanically polishing the layer of second material and the underlying layer of first material until the layer of first material is substantially planar to form a planarized layer of first material, the planarized layer of first material covering the wafer upper level of the top surface of the wafer; and forming a layer of third material on the planarized layer of first material, the third layer of material not contacting the wafer lower level and the wafer upper level see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

8. Claim 17 is rejected under 35 U.S.C. 102(e) as being anticipated by Doan et al. (US/6,331,488).

Re claim 17, Doan et al. disclose a method for forming a planarized layer of material on a processed wafer (see Fig. 7), the wafer (20) having a top surface, the top surface having spaced apart wafer (20) upper levels and a wafer lower level that lies between the wafer upper levels, the wafer upper levels lying above the wafer lower level, the method comprising the steps of forming a layer of first material (24) on the top surface of the wafer (20), the layer of first material (24) having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level; forming a layer of second

material (30) on the top surface of the layer of first material (24), the second layer of material (30) being thicker than the layer of first material (24); and chemically-mechanically polishing the layer of second material and the underlying layer of first material with a slurry until the layer of second material is substantially all removed from the layer of first material to form the planarized layer of material, the planarized layer of material lying over the wafer upper levels and the wafer lower level (see Figs. 4-7 and related text in Col. 7, line 14 – Col. 10, line 59).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. (US/6,162,368) in view of Weling et al. (US/5,378,318).

Re claim 9, Li et al. disclose a method for forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having spaced-apart wafer upper levels a wafer lower level that lies between the wafer upper levels, the wafer upper levels lying above the wafer lower level, the method comprising the steps of: forming a layer of first material (16) on the top surface of the wafer (10), the layer of first material (16) having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level; forming a layer of second material (60) on the top surface of the layer of first material (16); and chemically-mechanically polishing the layer of second material (18) and the underlying layer of first material (16) with a slurry until the layer of second material (18)

is all removed from the layer of first material (16) to form the planarized layer of material; and wherein the layer of first material makes an electrical contact with a device on the wafer, the planarized layer of material lying over the wafer upper levels and the wafer lower level (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

However, Li et al. do not specifically disclose the etch selectivity of the first material to the second material being 0.9-1.1:1.

Weling et al. disclose CMP of the first material (21) and second material (23) with a eth selectivity of 1:1, i.e., within the overlap range of the claimed limitation (see Fig. 1, Col. 7, lines 6-11).

Both Li et al. and Weling et al. teachings are directed to CMP process in order to planarize a material for semiconductor device fabrication. Therefore, the teachings Li et al. and Weling et al. are analogous

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Li et al. reference with etch selectivity ratio 1:1 as taught by Weling et al. because in order to polish the first layer and second layer at the same rate and form planar surface for the fabrication of semiconductor device.

Response to Arguments

11. Applicant's arguments with respect to claims 9, 17, 29 and 30 have been considered but are moot in view of the new ground(s) of rejection.

12. Applicant's arguments filed on January 30, 2004 have been fully considered but they are not persuasive.

With respect to new matter objection under 35 U.S.C. § 132, applicant argued that the specification in page 5, line 16 to page 6, line 1 provides support for the objected recitations. In response to applicant's argument, it is respectfully submitted that none of the added elements as set forth in Paragraphs 3 and 4 herein above have support in the specification as **the specification originally filed**. There is no implicit or explicit reference to third layer, i.e., layer **342** as a material being lowering (reducing) the resistance of the first layer **340** (i.e., the planar polysilicon layer). In addition, if the layer **342** considered to be the material that lower resistance of the polysilicon layer (i.e., for the sake of argument) such claim would have violated the rule that set forth under 35 U.S.C. § 112 first Paragraph for not having enabling disclosure for the material in question because there is no implicit, explicit or exemplary description of the type of the third material that would have ability to reduce the resistance of the polysilicon layer (i.e., the first material). Therefore, the objections under 35 U.S.C. § 132 is deemed proper.

With respect to the claims rejection under 35 U.S.C. § 112 1st Paragraph, applicant argued that the specification in page 5, line 16 to page 6, line 1 provides support for the rejected claims and the amendment do not introduce a new matter. In response to applicant's argument, it is respectfully submitted that none the rejected clams as shown in Paragraph 3 and 4 above have support in the specification as **the specification originally filed**. Therefore, the claims rejection under 35 U.S.C. § 112 first Paragraph is deemed proper.

With respect to claims rejection under 35 U.S.C. §102(e), applicant argued that "the first polishing step Li can not be read to be CMP polishing step of claim 1 because the first CMP step of Li does not form planarized layer material..."

In response to the applicant's argument, it is respectfully submitted that Li et al. disclose all the claimed limitations as applied in Paragraph 7 above. In addition, the rejected claim does not call for either single step or prularity step of CMP it just simply recites "chemically-mechanically polishing the layer of second material (330) and the underlying layer of first material (320) with a slurry until the layer of second material (330) is all removed from the layer of first material (320)." And Li et al. teaches that also. Whether one slurry used or multiple slurry utilized is irrelevant the rejected claim is not distinctive form the prior art. Furthermore, the term "until" does not have any special meaning to be construed by applicant as single CMP step process because the dictionary interpretation of "until" does not necessary preclude the intervening action. For example, applicant present "We walked until it got dark." For instance, the sentence didn't say they walked until it gets dark **without stopping or resting**. Among many reasons, the phrase "until" in the claim cannot be construed to as a single CMP process step without stopping.

The claims are given their broadest reasonable interpretation in light of the supporting disclosure. See *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

Applicant further argued that "Li fails to teach or suggest the formation of a layer of third material, claim 22 is not anticipated by the Li reference. In addition, since claims 19-21 and 23 depend from claim 22, claims 19-21 and 23 are not anticipated by Li for the same reasons as claim 22. With respect to claim 24, this claim recites, in part, selectively etching the planarized layer of material that covers the wafer upper levels and the wafer lower level of the top surface of the wafer." In rejecting claim 24, the Examiner stated, with reference to the selectively etching step, selectively etching the planarized layer of material that covers (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54)." Applicant respectfully has been unable to identify the steps in Li that the Examiner believes reads on the selectively etching step, and has been otherwise been unable to find any discussion in Li that teaches or suggests that polysilicon layer 16 (the layer of first material) is selectively etched when polysilicon layer 16 covers the upper levels of regions 14 as required by claim 24. As a result, claim 24 is not anticipated by Li. In addition, since claims 25 and 27-28 depend either directly or indirectly from claim 24, claims 25 and 27-28 are not anticipated by Li for the same reasons as claim 24..."

In response to the applicant's argument, it is respectfully submitted that Li et al. '368 disclose formation of the third layer (106) (see Fig. 2E). Furthermore, with respect to selectively etching step, the argument is moot because applicant fail to provide support for the limitation. However, Li et al. '368 also disclose the selectively etching step for the third material layer as shown in Figs. 2E and 2F. Therefore, the rejection under 35 U.S.C. §102(e) is deemed proper.

Conclusion

13. THIS ACTION IS MADE **NON-FINAL**.

Correspondence

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BK
February 20, 2005

George Fourson
Primary Examiner